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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
THORNEWELL, KIMBERLY A	
ART UNIT	**PAPER NUMBER**
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/26/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/736,386	WHITEFIELD ET AL.	
	Examiner	Art Unit	
	Kimberly Thornewell	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/27/05, 1/10/06, 7/6/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 have been presented for examination.

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on 10/27/2006, 1/10/2006 and 7/6/2006 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Claim Interpretation

3. Regarding claims 2-4, the mere ability for a method step to perform a function does not *necessitate* that the function be performed. Therefore, any prior art that does not prohibit the merging of values from different products meets the claim.

Since Phrase "can be" reads on undefinate function

Claim Objections

4. Claim 1 is objected to because step h reads defining a grid that is "at the resolution *of* needed for the analysis."

5. Claims 10-13 are objected to because the claims should read, "corresponding *to the* die site."

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the following limitations that contain insufficient antecedent basis:

- "one product/device," "virtual die coordinate" and "corresponding value" in step b.
- "die coordinate" in step c.
- "virtual die" and "composite value" in step d.
- "physical translation key" in step e.
- "files" in step g.
- "analysis" in step h.
- "wafer profile" in step l.

Furthermore, step h of claim 1 is directed to defining a grid that is at the "resolution needed" for analysis. The Applicant has not defined the requirements of a resolution to be used for analysis. Still furthermore, step l is directed to plotting the wafer profile for "various visualizations." The Applicant has not specifically described the visualizations to be plotted.

Regarding claim 7, the Applicant has not disclosed what constitutes a "sufficient" number of lots, or a "reasonable" average result.

Claim 19 recites the limitation "range of values" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Any rejected claims not specifically discussed are rejected by virtue of their dependence.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-2 and 5-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Jordan, III et al., US Patent no. 5,864,394.

As per claim 1,

Jordan discloses a method for calculating high-resolution wafer parameter profiles comprising the steps of:

a. Defining appropriate product/device input dataset (**column 10 lines 35-46**, *data gathering and sampling on a surface*);

b. Collecting a die level dataset for one of the products/devices defined in step (a) (**column 12 lines 37-43**) by generating a table of data for the lots and wafers of said one product/device with the virtual die (**column 12 lines 61-64**) coordinate for each die and

its corresponding value (*sweeping, collecting a value for each value in the sweep,* **column 12 lines 44-51**);

c. Calculating a single composite value for each die coordinate (**column 11 line 51-56**, *calculating intensity*);

d. Defining where on the virtual die it is desired to assign the composite value (**column 12 line 65-column 13 line 2,** *intensity and aligning the beam with the virtual pattern on the location to be sampled*);

e. Calculating physical coordinates for each die value using the corresponding virtual coordinate and physical translation key (**column 15 line 61-column 16 line 5,** *shows that coordinate locations are calculated for each intensity value*);

f. Repeating steps (b), (c), (d) and (e) for each product defined in step (a) (**column 14 lines 41-46**, *multiple events being processed*);

g. Merging the data from all the files into one file (**column 14 line 54**, *merging events*);

h. Defining a grid that is at the resolution needed for analysis (**column 10 lines 37-51**, *analyzes a grid having a resolution of sixteen pixels*);

i. Creating a table with all the possible grid coordinates that would fit on a production wafer (**column 25 line 47-column 26 line 6**, *generating convolution data given a wafer size*);

j. Defining a smoothing algorithm (**column 16 lines 58-61**, *interpolation exploiting smooth shape*);

k. Calculating the smoothed value for each point on the grid from the combined data (**column 16 lines 50-58**); and

l. Plotting the wafer profile for various visualizations (**figures 18 and 19**).

As per claim 2,

Jordan discloses normalizing the composite die values so that they can be merged with values from the other products (**column 11 lines 30-38**, *figure 1B, Gaussian distribution*).

As per claim 5,

Jordan discloses the appropriate product/device input dataset being defined by a variety of devices sizes (**column 12 lines 37-43**, *comparison of multiple strip units*) with die level data and different die sizes (**column 12 lines 52-61**, *different sizes of strip units*).

As per claim 6,

Jordan discloses the appropriate product/device input dataset being defined by products/devices which represent the same process flow to be modeled (**column 3 lines 54-64,** *finding intensities on all pixels*).

As per claim 7,

Jordan discloses the appropriate product/device input dataset being defined by a sufficient number of lots from each device to calculate a reasonable average result value for each die (**column 16 lines 36-39**).

As per claim 8,

Jordan discloses the appropriate product/device input dataset being defined by die size for each device (**column 12 lines 52-61**).

As per claim 9,

Jordan discloses the appropriate product/device input dataset being defined by at least one reference physical correlation point between a specific virtual coordinate and an actual physical location on the wafer (**column 12 line 65-column 13 line 2**).

As per claim 10,

Jordan discloses the calculated single composite value for each die coordinate being an average of the data from all the individual lots and wafers corresponding die site (**column 20 lines 6-11**).

As per claim 11,

Jordan discloses the calculated single composite value for each die coordinate being a max of the data from all the individual lots and wafers corresponding die site (**column 20 lines 33-37**).

As per claim 12,

Jordan discloses the calculated single composite value for each die coordinate being a sum of the data from all the individual lots and wafers corresponding die site (**column 25 lines 47-56**).

As per claim 13,

Jordan discloses the calculated single composite value for each die coordinate being a percentage of the data from all the individual lots and wafers corresponding die site (**column 17 lines 38-45**).

As per claim 14,

Jordan discloses the composite value being assigned to a corner of the die nearest an edge of the wafer (**column 9 lines 29-31**).

As per claim 15,

Jordan discloses the composite value being assigned to a corner of the die nearest a center of the wafer (**column 10 lines 12-14**).

As per claim 16,

Jordan discloses the composite value being assigned from a center of the die (**column 17 lines 5-8**).

As per claim 17,

Jordan discloses a Cartesian coordinate system being used to calculate physical coordinates (**column 12 lines 20-23**, *stage coordinate*).

As per claim 18,

Jordan discloses a polar coordinate system being used to calculate physical coordinates (**column 12 lines 20-23**, *wafer coordinate*).

As per claim 19,

Jordan discloses the wafer profile being scaled, in equal increments of the range of values (**column 19 lines 38-44**).

As per claim 20,

Jordan discloses the wafer profile being scaled in equal percentiles of the data (**column 25 lines 6-11**).

As per claim 21,

Jordan discloses the wafer profile being plotted to show a three-dimensional contour map of the data (**figure 7**).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jordan as applied to claims 1-2 and 5-21 above, in view of Misutake et al., US Patent no. 6,885,950.

Jordan does not disclose expressly a Poisson Defect Density normalizing algorithm being used to perform the step of normalizing the composite die values so that they can be merged with values from the other products. Mitsutake discloses a method for extracting wafer parameters including using a Poisson Defect Density normalizing algorithm to normalize the data so that they can be merged (**column 7 lines 14-23**).

It would have been obvious, at the time of the present invention, to modify Jordan's wafer extraction method with Mitsutake's Poisson Defect Density normalizing algorithm in order to normalize composite die value so they can be merged with values from different products. The motivation for doing so would have been to represent random defects within the extracted wafer parameter profiles (Mitsutake column 7 lines 36-63).

12. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jordan as applied to claims 1-2 and 5-21 above, in view of Maaya et al. US Patent no. 7,065,239.

Jordan does not disclose expressly a max-min scaling normalizing algorithm being used to perform the step of normalizing the composite die values so that they can be merged with values from the other products. Maaya discloses a method for extracting wafer parameters

including using a max-min scaling normalizing algorithm to normalize the data so that they can be merged (**column 14 lines 32-42**).

It would have been obvious, at the time of the present invention, to modify Jordan's wafer extraction method with Mitsutake's max-min scaling normalizing algorithm in order to normalize composite die value so they can be merged with values from different products. The motivation for doing so would have been to stabilize the range of parameters for a wafer (Maaya column 14 lines 42-44).

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly Thornewell whose telephone number is (571)272-6543. The examiner can normally be reached on 9am-5:30pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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KAT

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SUPERVISORY PATENT EXAMINER